If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

It is respectfully requested that any shortage in the fee be charged to the account of Antonelli, Terry, Stout & Kraus, LLP, Account No. 01-2135 (Case No. 843.39542X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By 

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"Version With Markings To Show Changes Made"

In the Claims:

Claims 1, 8, 11, 15, 16, 17, 19, 20 and 21 have been amended as follows:

1. (Amended) A semiconductor integrated circuit device [having] comprising: a semiconductor substrate of a first conductivity type; a zener diode [composed] comprised of a first semiconductor region of a second [electrically] [conducting] conductivity type formed in a primary face of [a] said semiconductor substrate [of a first electrically conducting type], and a second semiconductor region that is [a] of said first [electrically] [conducting] conductivity type [that is] formed in [the] said semiconductor substrate at a bottom portion of said first semiconductor region and [is] being smaller than said semiconductor region in an area surround a planar pattern thereof.

[the device comprising] wherein a plurality of first connection holes for electrically connecting said first semiconductor region and a wire to each other [wherein the first connection holes] are arranged in a region being outside a junction formed between said first semiconductor region and said second semiconductor region.

8. (Amended) A semiconductor integrated circuit device [having] comprising: a semiconductor substrate of a first

conductivity type; a zener diode [composed] comprised of a first semiconductor region of a second [electrically] [conducting] conductivity type formed in a primary face of [a] said semiconductor substrate [of a first electrically conducting type], and a second semiconductor region [that is a] of said first [electrically] [conducting] conductivity type [and is] formed in [the] said semiconductor substrate at a bottom portion of said first semiconductor region and [is] being smaller than said first semiconductor region in an area surrounding a planar pattern thereof,

[the device comprising] wherein a plurality of first connection holes for electrically connecting said first semiconductor region and a wire to each other [wherein said first connection holes] are arranged in a region being outside a junction formed between said first semiconductor region and said second semiconductor region, and wherein each of said plurality of first connection holes is spaced apart from [each] others of said connection holes so that a pitch between the adjacent first connection holes is greater than a maximum pitch between connection holes of the circuit.

11. (Amended) A semiconductor integrated circuit device comprising:

a plurality of first connection holes for electrically connecting a first wire and a first semiconductor region formed in a first region of a primary face of a semiconductor

substrate, to each other therethrough; and

a plurality of second connection holes for electrically connection a second wire and a second semiconductor region formed in a second region of the primary face of the semiconductor substrate, to each other therethrough, wherein each of said plurality of first connection holes is spaced from [each] others of said first connection holes so that a pitch between the adjacent first connection holes is greater than a minimum pitch between connection holes of the circuit, and wherein each of said plurality of second connection holes is spaced from [each] others of said second connection holes so that a pitch between [the] adjacent second connection holes [are about] substantially equal to the minimum pitch of the connection holes of the circuit.

15. (Amended) A semiconductor integrated circuit device comprising:

a first semiconductor region of a first [electrically] [conducting] conductivity type formed in a primary face of a semiconductor substrate;

a second semiconductor region of [a] said first [electrically] [conducting] conductivity type formed on said semiconductor substrate at an upper part of said first semiconductor region, [the] said second semiconductor region having a higher impurity concentration than said first semiconductor region;

a third semiconductor region of a second [electrically] [conducting] conductivity type formed in said semiconductor substrate at upper parts of said first and second semiconductor regions;

a first insulation film formed on [the] said primary face of said semiconductor substrate;

a first connection hole [that consists] comprised of a plurality of connection holes formed in said first insulation film at [the] said upper part of said first semiconductor region; and

a second connection hole [that consists] comprised of a plurality of connection holes formed in said first insulation film at [the] said upper part of said third semiconductor region, wherein said second connection hole is formed in an upper part of a region in which said first semiconductor region and said third semiconductor region from a junction.

16. (Amended) A semiconductor integrated circuit device according to claim 15, wherein a first [and second] electrically conductive connection bod[ies]y of said first conductivity type and a second electrically conductive connection body of said second conductivity type are provided inside said first and second connection holes, respectively, and wherein a first wire electrically connected to said first semiconductor region via said first electrically conductive connection body, and a second wire electrically connected to

said third semiconductor region via said second electrically connecting connection body are formed at [an] said upper part of said first insulation film.

17. (Amended) A semiconductor integrated circuit device according to claim 16, wherein said first semiconductor region is [composed] comprised of a fourth semiconductor region of [a] said first [electrically] [conducting] conductivity type, and a fifth semiconductor region electrically connected to said first electrically conductive connecting body via said fourth semiconductor region, [the] wherein an impurity concentration of said fifth semiconductor region [being] is lower than an impurity concentration of said fourth semiconductor region [in impurity concentration].

19. (Amended) A semiconductor integrated circuit device comprising:

a first semiconductor region formed in the primary face of a semiconductor substrate;

a second semiconductor region of a first [electrically] [conducting] conductivity type formed on said semiconductor substrate at an upper part of said first semiconductor region;

a third semiconductor region of a second [electrically] [conducting] conductivity type formed on said semiconductor substrate at upper parts of said first and second semiconductor regions;

a first insulation film formed on [the] said primary face of said semiconductor substrate;

a first connection hole [composed] comprised of a plurality of connection holes formed on said first insulation film at [the] said upper part of said first semiconductor substrate; and

a second connection hole [composed] comprised of a plurality of connection holes formed on said first insulation film at an upper part of said third semiconductor region, wherein a minimum pitch between [the] adjacent connection holes of said second connection hole is greater than [that] a minimum pitch between [the] adjacent connection holes of said first connection hole.

20. (Amended) A semiconductor integrated circuit device according to claim 19, wherein said first semiconductor region is a semiconductor region of [a] said second [electrically] [conducting] conductivity type and is lower than said second semiconductor region in a impurity concentration.

21. (Amended) A semiconductor integrated circuit device according to claim 19, wherein said first semiconductor region is a semiconductor region of [a] said second [electrically] [conducting] conductivity type that [configures] forms a collector region of a bipolar transistor, said second semiconductor region is a semiconductor region of [a] said

first [electrically] [conducting] conductivity type that [configure] forms a base region of said bipolar transistor, and said third semiconductor region is a semiconductor region of [a] said second [electrically] [conducting] conductivity type that [constitutes] forms an emitter region of said bipolar transistor.

Claims 22 and 23 have been added.